



## **REMARKS**

The drawings were objected to under 37 CFR 1.83(a). The examiner indicated that "the control circuitry connection to the input signal as recited in claim 1 must be shown . . ." The feature recited in old claim 1, and in new claims 26-55 is "control circuitry responsive to deviations of the PLL input signal's frequency. . ." The control circuitry detects such deviations in a variety of ways. For example, as illustrated in Figure 2 and described in the discussion related thereto, the control circuitry monitors such frequency deviations via a connection between the output of the A/D converter 120 and the control circuitry 105. Or, as illustrated in Figure 3 and described in the discussion related thereto, the frequency monitoring is achieved via a connection between the output of the phase comparator 106 and the beat detector 126. No connection between the input signal and the control circuitry is recited in the claims.

However, the limitation of "measuring the voltage of said control signal coupled to the oscillator" is included in the claims and it is assumed that this is the limitation to which the Examiner objected. Because the connection between the control circuitry 104 and the PLL circuitry 102 may be made in a variety of ways, the connection between the control signal coupled to the oscillator 110 and the out of range detector 112 in the higher-level conceptual block diagram of Figure 1 is indicated as a dotted red connection line in the proposed amendment to Figure 1. That is, the connection between the control circuitry 104 and the PLL circuitry 102 may be made, for example, between a beat detector 126 and the phase comparator 106 of Figure 3, between the digital output of the A/D converter 120 and the controller 105 of Figure 2, or between an out of range detector 112 and the control signal coupled to the oscillator 110. Consequently, the connection between line between the output of the filter 108 and the out-of-range detector 112 of Figure 1 is indicated as a dotted, rather than solid, line.

Claims 1, 9, and 20 were rejected under 35 U.S.C. 102 (e) as being anticipated by US Pat 5,903,748 (McCollough). Claims 2-8, 10-18 and 21- 25 were objected to as being dependent upon a rejected base claim, but were allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. All new claims 26 -29, 30-35, 36-39, 40-47, 48, 49-51, and 52-55 include all such limitations and, as such, should now be in form for allowance.

Claim 19 was rejected under 35 U.S.C. 103(a) as being unpatentable over McCollough in view of US Pat 5,719,508 (Daly). New claim 48, which replaces claim 19, includes the limitations of a phase-locked-loop as in allowable claim 30 and is therefore considered to be in form for allowance. All the claims are therefore believed to be allowable over the prior art of record for the same reasons discussed above with regard to the particular independent claim from which they depend. Consideration of Claims 26-55 is respectfully requested.

In light of the foregoing amendments and remarks, it is respectfully requested that all the claims be allowed such that the application may be passed to issue. If it is believed that a telephone conference will help expedite prosecution of the application, the examiner is invited to call the undersigned. The Commissioner is hereby authorized to charge any fees due for the filing of this paper, or to credit any refund, to applicants' Deposit Account No. 12-2325.

Respectfully submitted,

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## **REMARKS**

The examiner requested a copy of the 4/10/00 amendment. Due to printer problems at the time the original amendment was submitted, the document was replete with smudges which may have given the impression that several had been marked through. A "clean" copy of the amendment as filed is enclosed.

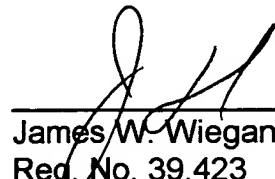
The examiner rejected claims 26-55 under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. The examiner maintains that it is unclear as to how the beat circuitry will detect deviations in the input frequency.

As noted at page 9, line 26 through page 11 line 5, when the frequency of the signal PLLin,  $F_i$ , (the "input frequency") exceeds the lock range of the PLL, the output state of the beat detector toggles at a frequency that is a function of 1) the instantaneous input frequency, 2) the instantaneous VCO frequency 3) a feedforward counter and 4) a feedback counter. The beat detector output, a function of the input frequency, is monitored by a beat evaluator. The time between transitions in the beat detector output is related to the frequency difference between an input signal and a reference signal (the difference between the PLL input signal and the VCO signal, in this case). That is, the time between transitions of the beat detector output provides a convenient measure of the difference between the instantaneous PLL input signal frequency and the instantaneous VCO signal frequency. Deviations in the time between transitions of the beat detector output will, therefore, provide an indication of the deviations in the input frequency. Such deviations may be employed, for example by the beat evaluator to enable the PLL to acquire lock, once the beat evaluator determines (as indicated by the time between beat detector transitions) that the instantaneous input frequency and the instantaneous VCO frequency are within an acceptable range of one another.

All the claims are therefore believed to be allowable over the prior art of record. Consideration of Claims 26- 55 is respectfully requested.

In light of the foregoing remarks, it is respectfully requested that all the claims be allowed such that the application may be passed to issue. If it is believed that a telephone conference will help expedite prosecution of the application, the examiner is invited to call the undersigned. The Commissioner is hereby authorized to charge any fees due for the filing of this paper, or to credit any refund, to applicants' Deposit Account No. 12-2325.

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